CLAIM AMENDMENTS

Claims 1-7 (cancelled).

Claim 8 (new): A circuit for downscaling a source image in both horizontal and vertical directions to generate a destination image, comprising:

an input processing unit, adapted for receiving said source image, providing image data at a first access frequency;

a horizontal direction image processing unit, electrically coupled to said input processing unit, receiving said image data at said first access frequency from said input processing unit and downscaling said image data in said horizontal direction to generate first temporary image data at said first access frequency;

a first stage line buffer unit, electrically coupled to said horizontal direction image processing unit, temporarily storing said first temporary image data at said first access frequency, wherein said first stage line buffer unit comprises a plurality of line buffers in series for periodic storing of said first temporary image data in each of said line buffers;

a vertical direction image processing unit, electrically coupled to said first stage line buffer unit, receiving said first temporary image data at said first access frequency from said first stage line buffer unit and downscaling said first temporary image data in said vertical direction to generate second temporary image data at said first access frequency;

a second stage line buffer unit, electrically coupled to said vertical direction image processing unit, temporarily storing said second temporary image data at said first access frequency; and

an output processing unit, electrically coupled to said second stage line buffer unit, reading said second temporary image data from said second stage line buffer unit at a second access frequency to generate said destination image.

Claim 9 (new): The circuit, as recited in claim 8, wherein said first stage line buffer unit is a first stage First-In-First-Out buffer unit comprising a plurality of First-In-First-Out buffers in series, wherein input terminals of said First-In-First-Out buffers are output terminals of said first stage line buffer unit.

Claim 10 (new): The circuit, as recited in claim 8, wherein said second stage line buffer unit is a second stage First-In-First-Out buffer.

Claim 11 (new): The circuit, as recited in claim 9, wherein said second stage line buffer unit is a second stage First-In-First-Out buffer.

Claim 12 (new): The circuit, as recited in claim 8, wherein said horizontal direction image processing unit comprises:

a horizontal direction data calculating element, electrically coupled to said input processing unit, receiving said image data at said first access frequency from said input processing unit and downscaling said image data in said horizontal direction to generate said first temporary image data at said first access frequency; and

a horizontal direction data controlling element, electrically coupled to said horizontal direction data calculating element, controlling said horizontal direction data calculating element to receive said image data at said first access frequency and to generate said first temporary image data at said first access frequency.

Claim 13 (new): The circuit, as recited in claim 11, wherein said horizontal direction image processing unit comprises:

a horizontal direction data calculating element, electrically coupled to said input processing unit, receiving said image data at said first access frequency from said input processing unit and downscaling said image data in said horizontal direction to generate said first temporary image data at said first access frequency; and

a horizontal direction data controlling element, electrically coupled to said horizontal direction data calculating element, controlling said horizontal direction data calculating element to receive said image data at said first access frequency and to generate said first temporary image data at said first access frequency.

Claim 14 (new): The circuit, as recited in claim 8, wherein said vertical direction image processing unit comprises:

a vertical direction data calculating element, coupled to said first stage line buffer unit, receiving said first temporary image data at said first access frequency from said first stage line buffer unit and downscaling said first temporary image data in said

vertical direction to generate said second temporary image data at said first access frequency; and

a vertical direction data controlling element, electrically coupled to said vertical direction data calculating element, controlling said vertical direction data calculating element to receive said first temporary image data at said first access frequency and to generate said second temporary image data at said first access frequency.

Claim 15 (new): The circuit, as recited in claim 9, wherein said vertical direction image processing unit comprises:

a vertical direction data calculating element, coupled to said first stage line buffer unit, receiving said first temporary image data at said first access frequency from said first stage line buffer unit and downscaling said first temporary image data in said vertical direction to generate said second temporary image data at said first access frequency; and

a vertical direction data controlling element, electrically coupled to said vertical direction data calculating element, controlling said vertical direction data calculating element to receive said first temporary image data at said first access frequency and to generate said second temporary image data at said first access frequency.

Claim 16 (new): The circuit, as recited in claim 13, wherein said vertical direction image processing unit comprises:

a vertical direction data calculating element, coupled to said first stage line buffer unit, receiving said first temporary image data at said first access frequency from said first stage line buffer unit and downscaling said first temporary image data in said vertical direction to generate said second temporary image data at said first access frequency; and

a vertical direction data controlling element, electrically coupled to said vertical direction data calculating element, controlling said vertical direction data calculating element to receive said first temporary image data at said first access frequency and to generate said second temporary image data at said first access frequency.

Claim 17 (new): A method for downscaling source image in both horizontal and vertical directions to generate destination image, comprising the steps of:

(a) receiving a source image and providing image data at a first access frequency;

(b) downscaling said image data in a horizontal direction to generate first temporary image data at said first access frequency;

(c) temporarily storing said first temporary image data at said first access frequency in a first stage line buffer unit, wherein said first stage line buffer unit comprises a plurality of line buffers in series for periodic storing of said first temporary image data in each of said line buffers;

(d) receiving said first temporary image data at said first access frequency from said first stage line buffer unit and downscaling said first temporary image data in a vertical direction to generate second temporary image data at said first access frequency;

(e) temporarily storing said second temporary image data at said first access frequency in a second stage line buffer unit; and

(f) reading said second temporary image data from said second stage line buffer unit at a second access frequency to generate a destination image.

Claim 18 (new): The method, as recited in claim 17, wherein said first stage line buffer unit is a first stage First-In-First-Out buffer unit comprising a plurality of First-In-First-Out buffers in series, wherein input terminals of said First-In-First-Out buffers are output terminals of said first stage line buffer unit.

Claim 19 (new): The method, as recited in claim 17, wherein said second stage line buffer unit is a second stage First-In-First-Out buffer.

Claim 20 (new): The method, as recited in claim 18, wherein said second stage line buffer unit is a second stage First-In-First-Out buffer.